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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/605,293	06/28/2000	DAVID L. CHAPEK	MIO-0037-VA	5927

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 12/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/605,293	Applicant(s) CHAPEK, DAVID L.	
	Examin r N. Drew Richards	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-12 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-12 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 June 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The specification is objected to for not complying with 35 U.S.C. 112, first paragraph. The specification has not been written so as to enable a person of ordinary skill in the art to form a source and drain in a substrate where the substrate comprises silicon dioxide, quartz, or glass. See page 10 lines 22-25 of the specification. The specification states that the source and drain can be formed by conventional doping techniques. However, the specification does not enable one of ordinary skill in the art to form a source and drain in an insulating substrate by doping. Doping an insulating substrate will not produce a conductive layer to be used as a source or drain. Conventional doping adds dopants to a semiconducting layer (i.e. silicon) to form areas of high conductivity. Conventional doping techniques do not add dopants to an insulating layer to form a conductive source or drain.

The specification also has not been written so as to enable a person of ordinary skill in the art to form a layer of polycrystalline silicon on silicon dioxide by thermal oxidation. See page 8 line 12, page 9 line 21, page 13 line 21 and page 14 line 15. Thermal oxidation is a process in which an oxide layer is grown by the oxygen reacting with the starting material. It is not enabled how thermal oxidation can be used to form a layer of polycrystalline silicon on silicon dioxide as thermal oxidation adds oxygen to the layer. A thermal oxidation process performed on a layer of silicon dioxide would be understood in the art to produce more oxide from the underlying silicon and thicken the

silicon dioxide. It is not enabled how the oxygen is removed from the layer of silicon dioxide during thermal oxidation to provide polycrystalline silicon.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 9-12 and 14 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 9-12 and 14 include the limitation of the layer of silicon dioxide being free of metal contaminants. This limitation is indefinite. It is indefinite as to what is meant by "free of metal contaminants." Being "free of metal contaminants" can mean having no metal atoms at all, not having metal atoms of a certain species (but which may include metal atoms of other species), not having metal atoms above a certain concentration, or having metal atoms of a sufficiently low concentration so as to enable the structure to operate as intended. The limitation is unclear and indefinite because one cannot ascertain the metes and bounds of the limitation. If "free of metal contaminants" is interpreted to mean that there are some contaminants present, the limitation is indefinite as the specification does not objectively define what level of metal contaminants are considered "free of metal contaminants."

Claim 10 is further indefinite as it is unclear as to whether the gate oxide of line 10 is the same oxide as claimed in line 3 or whether a second oxide layer is claimed.

Claim 11 is further indefinite as it is unclear as to whether the gate oxide of line 13 is the same oxide as claimed in line 3 or whether a second oxide layer is claimed.

Claim 12 is further indefinite as it is unclear as to whether the series of gate oxides of line 12 is the same oxide as claimed in line 4 or whether a second oxide layer is claimed.

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 9-12 and 14 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 9-12 and 14 include the limitation of the layer of silicon dioxide being free of metal contaminants. This limitation is not enabled by the specification. It is not enabled as to how many metal contaminants or what species of metal contaminants can be present to be considered "free of metal contaminants." If "free of metal contaminants" is interpreted as meaning that there are zero metal atoms in the layer, atomic physics principles dictate that at least some metal contaminants will be present and the specification does not enable how one would form the claimed device with no metal contaminants. In the art, some level of metal contamination is known to necessarily be present in all devices. It is known that metal contaminants come from

many different sources including, but not limited to, metal chambers used in processing, metal pipes that gases flow through, and in the starting semiconducting substrates themselves.

6. As best understood, the claims are rejected as follows. For the art rejections below, "free of metal contaminants" is interpreted as meaning having metal atoms of a sufficiently low concentration so as to enable the structure to operate as intended.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 9 is rejected under 35 U.S.C. 102(a) as anticipated by Applicant's admitted prior art.

Applicant's admitted prior art discloses on page 1 lines 12-16 a semiconductor substrate, a layer of silicon dioxide on the substrate, and a layer of polycrystalline silicon formed on the silicon dioxide, the polycrystalline silicon having a smooth morphology. The admitted prior art discloses the layer of silicon dioxide having been doped with hydrogen ions. The semiconductor substrate is considered as a bottom portion of the silicon dioxide layer with the remaining silicon dioxide layer as the silicon dioxide layer upon the substrate. Though the admitted prior art does not explicitly state a layer of polysilicon is on the silicon dioxide it is implicitly understood that the polysilicon is formed seeing that the admitted prior art discusses performing the hydrogen doping of the silicon dioxide so as to provide a thinner, smoother polysilicon film deposited on the silicon dioxide. The admitted prior art does not explicitly state the layer of silicon dioxide being "free of metal contaminants" but this limitation is considered implicitly understood. The prior art discloses the use of hydrogen ion pretreatment of silicon dioxide to produce thinner and smoother polysilicon films and also discloses 64 Mb DRAMs. It is assumed that in forming the 64 Mb DRAMs the devices formed therein are operational and that the DRAMs discussed employ the hydrogen ion pretreatment. Thus, in interpreting the claim language "free of metal contaminants" to mean having metal atoms of a sufficiently low concentration so as to enable the structure to operate as intended, the admitted prior art discloses "free of metal contaminants" since the admitted prior art forms operational devices.

10. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burns et al. (Principles of Electronic Circuits, Pp. 380 and 381) in view of Applicant's admitted prior art.

Burns et al. teach a field effect transistor in figure 9.8 on page 381. Burns et al. teach a substrate, silicon dioxide layer, a layer of polycrystalline silicon over the silicon dioxide layer, and a gate oxide, a source and a drain in the substrate where a gate electrode is formed from the layer of polycrystalline silicon. Burns et al. do not teach the layer of silicon dioxide having hydrogen ions implanted therein or being free of metal contaminants. Applicant's admitted prior art teaches implanting hydrogen ions into silicon dioxide on page 1 lines 12-16. Applicant's admitted prior art as discussed above also teaches the silicon dioxide as being "free of metal contaminants."

Burns et al. and Applicant's admitted prior art are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the silicon dioxide layer. The motivation for doing so is to prepare the surface of the silicon dioxide for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. Therefore, it would have been obvious to combine Burns et al. with Applicant's admitted prior art to obtain the invention of claim 10.

With regard to claim 11, Burns et al. teach on pages 380 and 381, a memory array which further includes a plurality of memory cells arranged in rows and columns comprising at least one field effect transistor having a gate oxide, source, and drain

formed on the substrate and a gate electrode for each transistor formed of the layer of polycrystalline silicon.

With regard to claim 12, Official Notice is taken that one of ordinary skill in the art at the time of the invention would form the transistor of claim 10 or the memory array of claim 11 on a semiconductor wafer including a plurality of die. This is well known as in semiconductor processing multiple devices are formed on a single wafer then split into individual die to allow for processing of a great number of die at one time to save of processing costs. Also, the gate electrode is a repeating series of gate electrodes for each transistor on each die formed from the layer of polycrystalline silicon.

11. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murata et al. (U.S. Patent No. 5576229) in view of Applicant's admitted prior art.

Murata et al. teach a thin film transistor in figure 6E comprising a semiconductor substrate of glass, a layer of polycrystalline silicon 507 formed on a portion of the substrate, a insulating layer 503 formed on a portion of the polycrystalline silicon, a agte oxide, a source region 507a and drain region 507b formed in the polycrystalline silicon, and a gate electrode 504 formed on the insulating layer. Murata et al. do not teach the substrate having hydrogen ions implanted therein or the substrate being free of metal contaminants. Applicant's admitted prior art teaches implanting hydrogen ions into a silicon dioxide (glass) layer to provide a smooth topology polycrystalline silicon film thereon on page 1 lines 12-16. Applicant's admitted prior art as discussed above also teaches the silicon dioxide as being "free of metal contaminants."

Murata et al. and Applicant's admitted prior art are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to implant hydrogen ions into the glass substrate. The motivation for doing so is to prepare the surface of the glass substrate for the deposition of a layer of polycrystalline silicon to provide for a thinner and smoother polycrystalline silicon film. Therefore, it would have been obvious to combine Murata et al. with Applicant's admitted prior art to obtain the invention of claim 14.

Response to Arguments

12. Applicant's arguments filed 11/12/02 have been fully considered but they are not persuasive.

Applicant has argued that the specification has given written description to enable a source and drain formed in a silicon dioxide, glass, or quartz substrate and forming polycrystalline silicon on silicon dioxide by thermal oxidation. This is not persuasive. First, the specification does state that the source and drain can be formed by conventional doping techniques. However, the rejection arises from the fact that conventional doping techniques do not provide for adding dopants to an insulating substrate to form conductive regions. Conventional doping techniques used to form source and drain regions are performed on a semiconductor substrate (i.e. silicon, silicon carbide, gallium arsenide), not on an insulating substrate. Thus, one of ordinary skill in the art at the time of the invention would not know how to form the source and drain in an insulating substrate based on the specification. Also, even if doping did form

conductive regions those regions would not act as a source and drain because there would exist no semiconductive channel in between to allow transistor operation.

Second, polycrystalline silicon is not formed on silicon dioxide by thermal oxidation. Conventional thermal oxidation techniques introduce oxygen atoms into the substrate to grow an oxide. In the case of a silicon substrate, oxygen reacts with the silicon surface to produce silicon dioxide. Even if a layer of silicon dioxide is already formed on the silicon substrate, oxidation will grow a further oxide. For polycrystalline silicon to be formed from silicon dioxide one would have to remove the oxygen, the opposite of what occurs during oxidation. The specification does not enable how one ordinary skill in the art would remove the oxygen to form a polycrystalline silicon layer from silicon dioxide.

Applicant has made further arguments in regards to the previous 35 USC 103 rejections, however, these arguments are moot in view of the new grounds of rejection presented above.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (703) 306-5946. The examiner can normally be reached on M-F 8:00-5:30; Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

NDR
December 11, 2002